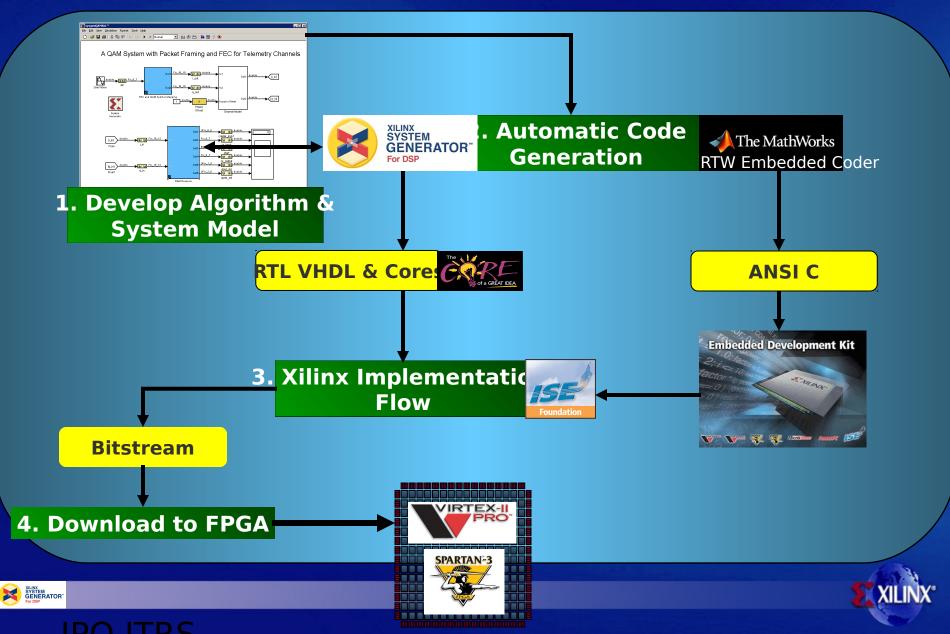


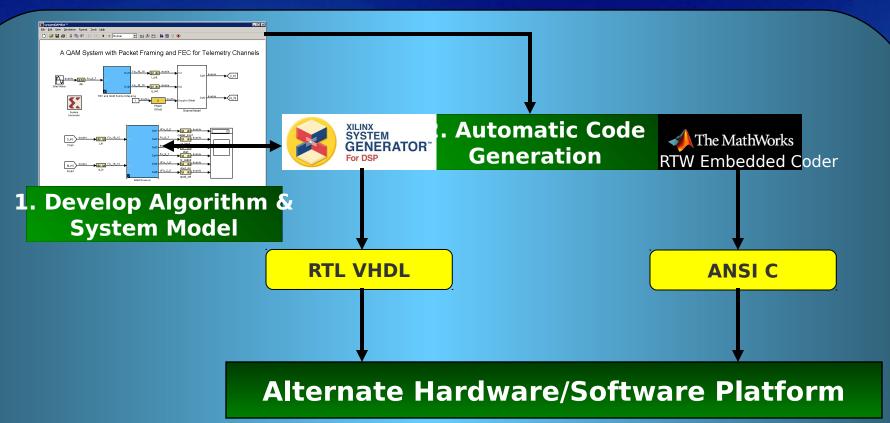
Using Simulink/System Generator for SDR Signal Processing Subsystems

JTRS JPO Technical Workshop on DSP and FPGA Portability 29 Jbo Hyprib 2004 Dr. Chris Dick Xilinx, Inc.

Platform FPGA Deployment



Retargeting the Design







SPS Function Interfaces

- Layered component portability for trading-off mobility vs. cost/performance
 - Waveform portable across FPGA/DSP/GPP based platforms
 - Different realizations of individual SPS functions may have variable mobility
 - AGC, DDC, DUC, Equalization, Carrier Recovery, Timing Recovery, FEC
 - High-level control and supervisory functions may have limited mobility
 - CORBA does not make sense at the level of a DDC
 - Function signatures define the narrowest compliant, and can be extended
 - · Clock signals, bus interfaces should be optional
 - Implementation options controllable through
 - Hierarchical decomposition
 - System level attributes
- Hardware interface guidelines
 - Flow control and synchronization
 - Should be composable through self-synchronizing circuitry (GALs)
 - Retargetable functions require a granularity where self-synchronization is efficient and cheap
 - Port interfaces and functional description
 - Input/output relation, latency or real-time constraints, spectral mask, etc.





Summary

- Platform-based design methodologies facilitate FPGA signal processing (COTS tools)
 - System specification and modeling
 - Simulink framework and language
 - Automatic code generation of hardware and firmware
 - System Generator for FPGA design of the SPS
 - Real-Time Workshop/Embedded Coder for firmware
- Need to establish hardware interfaces for data transport and control to support SPS function portability
 - Standardization a possibility, but will take time
 - Establishing guidelines and adopting recommendations in advance will be expedient
 - A good handshake goes a long way



